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T. Steptoe
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ASA-1062

jc929 U.S. PTO
10/073312
02/13/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

T. SASAKI et al

Serial No.

Filed: February 13, 2002

For: DESIGN METHOD AND SYSTEM FOR SEMICONDUCTOR INTEGRATED CIRCUITS

INFORMATION DISCLOSURE STATEMENT (IDS) UNDER § 1.97 AND § 1.98

Commissioner for Patents
Washington, D.C. 20231

Sir:

1. This IDS should be considered:

(a) when filed within three months of the filing date of the present application, or within three months of the filing date of the National Stage as set forth in § 1.491 in an international application, or before the mailing date of a first Office Action on the merits, whichever occurs last;

(b) when filed before the mailing date of either a Final Rejection under § 1.113 or a Notice of Allowance under § 1.311, whichever occurs first and when 1(a) does not apply. For this purpose, there is included herein either a certification in section 4 below (included when indicated by a marked box), or a fee of $180.00 (a check in the amount of $180.00 is enclosed, or if not see section 5 below);

(c) when filed prior to the payment of the Issue Fee, when 1(a)-(b) do not apply, and when a certification is included in section 4 below (included when indicated by a marked box); then the Applicant(s) hereby petition(s) and request(s) consideration of this IDS, and provided herewith is a fee of $180.00 (a check in the amount of $180.00 to cover the petition fee, or if not see section 5 below).

2. When 1(a)-(c) do not apply, then it is requested that this IDS be placed in the file.

3. Listing of the information submitted is on the attached Form PTO-1449, which forms a part of this IDS. A copy of each listed document is enclosed.

4. If a fee or additional fee is required, the Commissioner is hereby authorized to charge any fee or additional fee that may be required and credit any excess to Deposit Account No. 50-1417.

5. No explanation of relevancy is being provided for the documents because each is discussed in the present Specification.

6. If the PTO determines that part(s) of the required content is inadvertently omitted, then it is requested that the Applicant(s) be given additional time and specific identification of such omission(s) to enable full compliance.

Respectfully submitted,

John R. Mattingly
Registration No. 30,293
Attorney for Applicants

MATTINGLY, STANGER & MALUR
1800 Diagonal Rd., Suite 370
Alexandria, Virginia 22314
(703) 684-1120
Date: February 13, 2002

FORM PTO-1449 (REV. 7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. ASA-1062	SERIAL NO.
LIST OF DOCUMENTS CITED BY APPLICANT *(Use several sheets if necessary)*		APPLICANT T. SASAKI et al	
		FILING DATE February 13, 2002	GROUP

U.S. PATENT DOCUMENTS

* EXAMINER INITIAL		DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE *(If Appropriate)*
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

		DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AL						☐	☐
	AM						☐	☐
	AN						☐	☐
	AO						☐	☐
	AP						☐	☐

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, etc.)*

	AR		A. Takahashi et al, "Performance and Reliability Driven Clock Scheduling of Sequential Logic Circuits", Proceedings of the ASP-DAC '97, 1997, pp. 37-42.
	AS		K. Inoue et al, "Schedule-Clock-Tree Routing for Semi-Synchronous Circuits", Technical Report of IEICE, CAD21, 1998, pp. 54-61.
	AT		

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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